

10  
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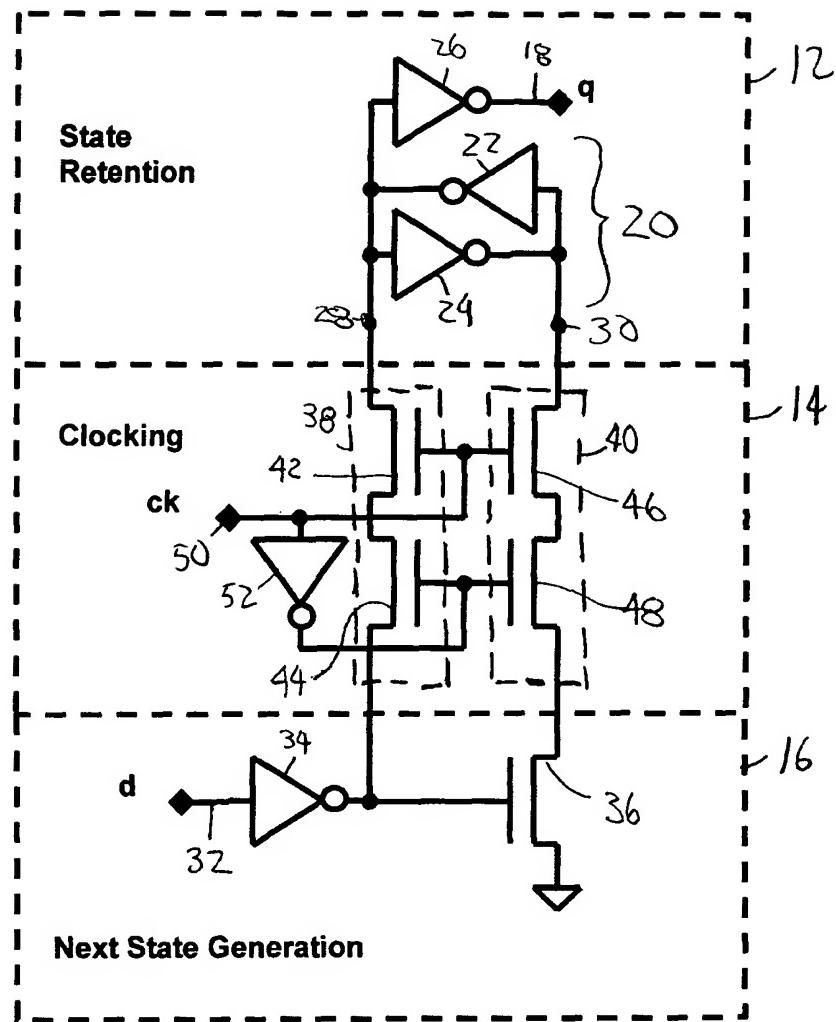


FIG. 1

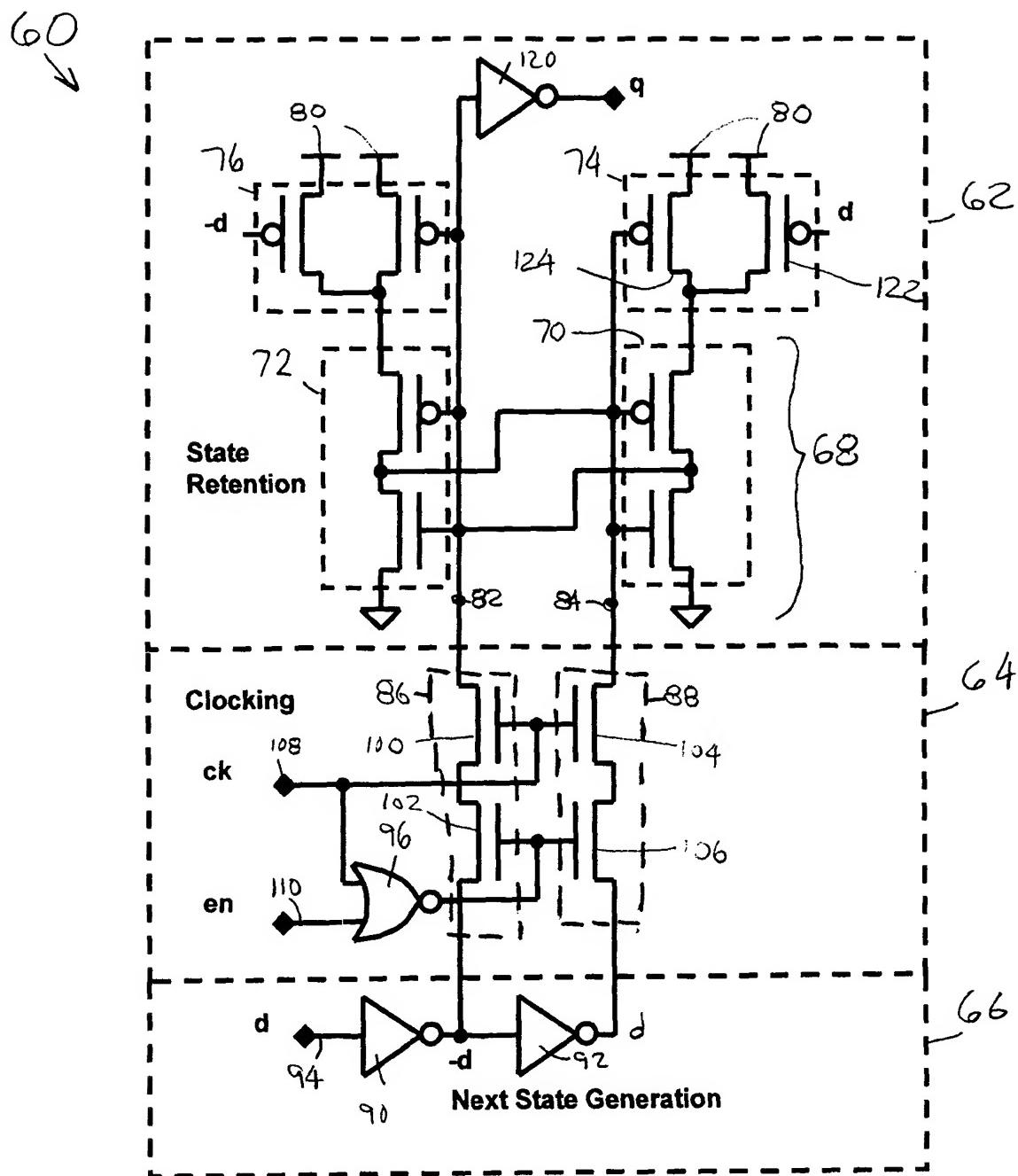


FIG. 2

130  
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PROVIDE A MEMORY CELL HAVING FIRST AND SECOND  
COMPLEMENTARY STORAGE NODES

132

PROVIDE A FIRST TRANSISTOR STACK COUPLED TO THE  
FIRST STORAGE NODE, THE FIRST TRANSISTOR STACK  
HAVING FIRST AND SECOND TRANSISTORS

134

PROVIDE A SECOND TRANSISTOR STACK COUPLED TO THE  
SECOND STORAGE NODE, THE SECOND TRANSISTOR STACK  
HAVING THIRD AND FOURTH TRANSISTORS

136

TURN ON THE FIRST AND THIRD TRANSISTORS AT A FIRST  
INSTANT IN TIME

138

TURN OFF THE SECOND AND FOURTH TRANSISTORS  
SHORTLY AFTER THE FIRST INSTANT IN TIME

140

Fig. 3